

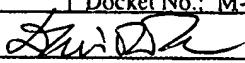
U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.	Serial No.
		M-15222 US	10/632,155
O INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		Applicant	
SEP 7 2003 U.S. PATENT AND TRADEMARK OFFICE		Yi Ding	
		Filing Date	Group
		July 30, 2003	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
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	AM						
	AN						
	AO						
	AP						
	AQ						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	United States Patent Application No. 10/440,466, entitled "Fabrication Of Conductive Gates For Nonvolatile Memories From Layers With Protruding Portions," Filed on May 16, 2003; Attorney Docket No.: M-12979 US.
	AS	United States Patent Application No. 10/440,005, entitled "Fabrication of Dielectric On A Gate Surface To Insulate The Gate From Another Element Of An Integrated Circuit," Filed on May 16, 2003; Attorney Docket No.: M-15203 US.
	AT	United States Patent Application No. 10/440,508, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories Having Select, Floating And Control Gates," Filed on May 16, 2003; Attorney Docket No.: M-15204 US.
	AU	United States Patent Application No. 10/440,500, entitled "Integrated Circuits With Openings that Allow Electrical Contact To Conductive Features Having Self-Aligned Edges," Filed on May 16, 2003; Attorney Docket No.: M-15205 US.

Examiner  Date Considered

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
<i>pw</i>	AV	United States Patent Application No. 10/393,212, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on March 19, 2003; Attorney Docket No.: M-12902 US.	
	AW	United States Patent Application No. 10/411,813, entitled "Nonvolatile Memories With A Floating Gate Having An Upward Protrusion," Filed on April 10, 2003; Attorney Docket No.: M-12903 US.	
	AX	United States Patent Application No. 10/393,202, entitled "Fabrication of Integrated Circuit Elements In Structures With Protruding Features," Filed on March 19, 2003; Attorney Docket No.: M-15151 US.	
	AY	United States Patent Application No. 10/631,941, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate," Filed on July 30, 2003; Attorney Docket No.: M-15171 US.	
	AZ	United States Patent Application No. 10/632,007, entitled "Arrays Of Nonvolatile Memory Cells Wherin Each Cell Has Two Conductive Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15223 US.	
	BA	United States Patent Application No. 10/631,452, entitled "Fabrication Of Dielectric For A Nonvolatile Memory Cell Having Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15229 US.	
	BB	United States Patent Application No. 10/632,154, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Mutiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15230 US.	
	BC	United States Patent Application No. 10/631,552, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on July 30, 2003; Attorney Docket No.: M-12902-1P US.	
<i>pw</i>	BD	United States Patent Application No. 10/632,186, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate And Having Upward Protrusions," Filed on July 30, 2003; Attorney Docket No.: M-15241 US.	
	BE		
	BF		
	BG		
	BH		
Examiner	<i>Stan R</i>	Date Considered	<i>6/7/06</i>
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DP	AS 6,437,360	20 Aug. 2002	Cho et al.			
	AT 6,438,036	20 Aug. 2002	Seki et al.			
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	BB 6,541,829	1 Apr. 2003	Nishinohara et al.			
DA	BC 6,414,872	2 Jul. 2002	Bergemont et al.			
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	BE	Kim, K.S. et al. "A Novel Dual String NOR (DuSnor) Memory Cell Technology Scalabe to the 256 Mbit and 1 Gbit Flash Memories," 1995 IEEE 11.1.1-11.1.4				
	BF	Bergemont, A. et al. "NOR Virtual Ground (NVG)- A New Scaling Concept for Very High Density FLAS EEPROM and its Implementation in a 0.5 um Process," 1993 IEEE 2.2.1-2.2.4				
DA	BG	Van Duuren, Michiel et al., "Compact poly-CMP Embedded Flash Memory Cells For One or Two Bit Storage," Philips Research Leuven, Kapeldreef 75, B3001 Leuven, Belgium, pages 73-74.				
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	BI					
	BJ					
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		Filed Herewith	Unassigned

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	AB 5,856,943	5 Jan. 1999	Jenq			
	AC 6,057,575	2 May 2000	Jenq			
	AD 6,130,129	10 Oct. 2000	Chen			
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✓	AJ 6,355,524	12 Mar. 2002	Tuan et al.			
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	AM	Naruke, K.; Yamada, S.; Obi, E.; Taguchi, S.; and Wada, M. "A New Flash-Erase EEPROM Cell with A Sidewall Select-Gate On Its Source Side," 1989 IEEE, pages 604-606.
	AN	Wu, A.T.; Chan T.Y.; Ko, P.K.; and Hu, C. "A Novel High-Speed, 5-Volt Programming EPROM Structure With Source-Side Injection," 1986 IEEE, 584-587.
	AO	Mizutani, Yoshihisa; and Makita, Koji "A New EPROM Cell With A Sidewall Floating Gate For High-Density and High Performance Device," 1985 IEEE, 635-638.
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	AQ	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 120-121.
✓	AR	Ma, Yale et al., "A Dual-Bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single Vcc High Density Flash Memories," 1994 IEEE, 3.5.1-3.5.4.

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